CLAIMS

1. A method of making a microelectronic assembly, comprising:

(a) providing a plurality of microelectronic packages;

(b) providing a support having a plurality of recesses, the support carrying a conductive element having a plurality of depressions, at least some of the depressions being disposed in a recess;

(c) assembling the conductive element with the microelectronic packages;

(d) removing the support after said assembling step; and

(e) severing the conductive element between the depressions to form individual conductive members for each microelectronic package.

2. The method of claim 1, wherein the support comprises a mandrel having a plurality of recesses corresponding to the depressions in the conductive element.

3. The method of claim 2, wherein the step of providing a support comprises depositing a conductive material on a surface of the support.

4. The method of claim 3, wherein the surface of the support comprises a material that does not adhere to the conductive material.

5. The method of claim 4, wherein the support comprises a material selected from the group consisting of molybdenum, steel, brass, and chromium.

6. The method of claim 5, wherein the conductive material comprises a material selected from the group consisting of copper, nickel, and gold.

7. The method of claim 2, wherein the step of providing the support comprises providing a metal mandrel with recesses.

8. The method of claim 2, wherein the recesses have a depth of about the depth of the package.

9. The method of claim 1, further comprising attaching bonding material to the conductive element.

10. The method of claim 9, further comprising attaching the conductive element to connection pads of another microelectronic element using the bonding material.

11. The method of claim 1, wherein each of said plurality of package comprises a semiconductor chip attached to a dielectric layer having terminal structures thereon and leads connecting to the chip and the terminal structures.

12. The method of claim 1, further comprising introducing a flowable material into said depressions.

13. The method of claim 12, wherein the conductive element defines bottom walls and side walls protruding forwardly from said bottom walls so that said walls cooperatively define said depressions, said side walls defining at least one pathway extending between adjacent ones of said depressions, said step of introducing a flowable material being performed so that said flowable material passes between at least some adjacent depressions through said pathways.

14. The method of claim 13, wherein each said package includes a semiconductor chip having an operating frequency and each said pathway has dimensions less than the wavelength of electromagnetic radiation at said operating frequency.

15. The method of claim 13, wherein said side walls are hollow and define wall spaces open to a rear wall of said conductive element, said at least one pathway communicating with said wall spaces, said step of removing said support being performed before said step of introducing said flowable material into said depressions, the method further comprising provided a rear covering layer overlying said rear walls of said depressions so that said rear covering layer blocks flow of said flowable material from said wall spaces onto exterior surfaces of said bottom walls.

16. The method of claim 12 wherein said step of

introducing said flowable material is performed before said step of removing said support.

17. A microelectronic assembly comprising:

(a) a conductive element including a bottom wall and a plurality of side walls extending from said bottom wall so that said bottom wall and said side walls define a depression, said conductive element having one or more additional openings in at least one of said walls;

(b) a dielectric layer extending between said side walls, so that said dielectric layer and said conductive element substantially enclose an interior space within said depression and said one or more openings in said conductive element communicate with said interior space;

(c) a microelectronic element disposed within said interior space; and

(d) an encapsulant including an interior portion at least partially filling said interior space and at least partially surrounding said microelectronic element within said space, and an exterior portion exposed at an exterior surface of said conductive element in contact with said conductive element, said portions of said encapsulant being connected to one another through said one or more additional openings in said conductive element.

18. An assembly as claimed in claim 17 wherein said side walls define said one or more additional openings.

19. An assembly as claimed in claim 18 wherein said exterior portion at least partially covers one or more of said side walls.

20. An assembly as claimed in claim 17 wherein said exterior portion of said encapsulant does not extend on said rear wall.

21. An assembly as claimed in claim 20 wherein said dielectric element has one or more terminal structures thereon electrically connected to said microelectronic element and said exterior portion of said dielectric does not extend onto said terminal structures.

22. An assembly as claimed in claim 17 wherein said side wall portions include a plurality of pillars spaced apart from one another, said one or more additional openings including spaces between adjacent ones of said pillars, said exterior portion of said encapsulant defining

23. An assembly as claimed in claim 22 wherein said microelectronic element is adapted to operate at an operating frequency and said one or more additional openings have dimensions less than a wavelength of electromagnetic radiation at said operating frequency.

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